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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,819	02/25/2004	Belgacem Haba	TESSERA 3.0-336 II	5082

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TESSERA
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WESTFIELD, NJ 07090

EXAMINER	
CAO, PHAT X	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,819	HABA ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) *3,15-19,27,28,30,33 and 44-68* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-14,20-26,29,31,32 and 34-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/04&10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election of species III (claims 1, 2, 4-14, 20-26, 29, 31-32, and 34-43) in the reply filed on 2/2/06 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-2, 4-14, 20-26, 29, 31-32, and 34-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoneda et al (US. 6,376,921).

Regarding claims 1-2 and 31-32, Yoneda (Fig. 132A) discloses a packaged chip comprising: a chip 311 having front and rear surfaces and contacts 312 (not labeled in Fig. 132A, see Fig. 132B) on the front surface; a coherent, self-supporting chip carrier

attached to the chip 311, the chip carrier including a dielectric layer 317 extending across one surface of the chip 311 and having an inner surface facing upwardly and an outer surface facing downwardly, the chip carrier having conductive traces 3151 thereon electrically connected to the contacts 312 and conductive bumps 315 formed integrally with the traces 3151, the conductive bumps 315 projecting downwardly from the traces, the bumps 315 having bottom ends exposed at the outer surface of the dielectric layer 317 for bonding to contact pads on a circuit panel 250 (not shown in Fig. 132A, see Fig. 85 and column 38, lines 58-60), wherein each of the bumps 315 has a first wall portion extending downwardly from one of the traces 3151, a bottom wall portion joining the first wall portion adjacent the bottom end of the bump, and a second wall portion extending upwardly from the bottom wall portion to the dielectric layer 317.

Regarding claims 4-5 and 34-36, Yoneda (Fig. 132A) further discloses that each of the bumps 315 is generally cup-shaped, with a closed end of the cup shape defining the bottom end of the bump and an open end of the cup shape facing upwardly, the cup-shaped bump 315 further has an imperforate sidewall extending upwardly from the bottom end of the bump 315 to the dielectric layer 317.

Regarding claims 6-8 and 37-39, Yoneda (Fig. 132A) also discloses that each bump 315 is substantially solid (i.e., metallic film), has an exterior surface in the form of a surface of revolution about a vertical axis, and has a lead-in surface sloping upwardly and outwardly around the entire periphery of the bump adjacent the bottom end of the bump.

Regarding claims 9, 11-12, and 40, Yoneda further discloses that all of the bumps 315 are disposed beneath the chip 311 (see Fig. 132A) and are disposed in one or more rows (see Fig. 132B) at a pitch of approximately equal to 0.8 mm (column 27, lines 35-36).

Regarding claims 10, 13-14, 29, and 41-43, Yoneda (Fig. 132A) further discloses that: the dielectric layer 317 extends beneath the chip 311 and the inner surface of the dielectric layer 317 faces upwardly toward the chip 311; the traces 3151 are disposed on the inner side and above the outer side of the dielectric layer 317; and the bumps 315 extend at least partially through the dielectric layer 317 and have bottom ends disposed below the outer surface of the chip carrier.

Regarding claims 20-21 and 25-26, Yoneda (Fig. 132A) further discloses that: the upwardly-facing bonding pads on the chip carrier 317 are electrically connected to the traces 3151 and bond wires 313 connect the bonding pads to the contact 312; and a spacer layer 316 of compliant resin (column 38, lines 6-10) is disposed between the chip 311 and the dielectric layer 317.

Regarding claims 22-24, Yoneda further discloses that the resin projections 318 can absorb a curvature of the resin package 314 when the device 310B is mounted on a circuit board (column 38, lines 58-60). Therefore, because the conductive bumps 315 are formed on the absorbing resin projections 318, the bottom ends of the conductive bumps 315 would be movable in a vertical direction or a horizontal direction when the bumps are mounted on a circuit board.

4. Claims 1-2, 4-8, 10-14, 29, 31-32, 34-39, and 41-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin (US. 6,660,626).

Regarding claims 1-2 and 31-32, if Figs. 1B and 1C of Lin are inverted, then Lin (Figs. 1B and 1C) discloses a packaged chip comprising: a chip 110 having front and rear surfaces and contacts 116 on the front surface; a coherent, self-supporting chip carrier attached to the chip 110, the chip carrier including a dielectric layer 126 extending across one surface of the chip 110 and having an inner surface 124 facing upwardly toward the chip 110 and an outer surface 122 facing downwardly away from the chip 110, the chip carrier having conductive traces 136 thereon electrically connected to the contacts 116 (see Fig. 1G) and conductive bumps 138 formed integrally with the traces 136, the conductive bumps 138 projecting downwardly from the traces 136, the bumps having bottom ends 142 exposed at the outer surface of the dielectric layer 126 for bonding to contact pads on a PCB circuit panel (not shown in Fig. 1C, see column 4, lines 16-24), wherein the bump 138 has a first wall portion extending downwardly from the trace 136, a bottom wall portion joining the first wall portion adjacent the bottom end 142 of the bump, and a second wall portion extending upwardly from the bottom wall portion to the dielectric layer 126.

Regarding claims 4-5 and 34-36, Lin (Fig. 1C) further discloses that the bump 138 is generally cup-shaped, with a closed end of the cup shape defining the bottom end 142 of the bump and an open end 128 of the cup shape facing upwardly, the cup-shaped bump 138 further has an imperforate sidewall extending upwardly from the bottom end 142 of the bump 138 to the dielectric layer 126.

Regarding claims 6-8 and 37-39, Lin (Fig. 1C) further discloses that the bump 138 is substantially solid, has an exterior surface in the form of a surface of revolution about a vertical axis, and has a lead-in surface sloping upwardly and outwardly around the entire periphery of the bump adjacent the bottom end 142 of the bump.

Regarding claims 11-12, Lin (Fig. 1C) further discloses that all of the bumps 138 are disposed beneath the chip 110.

Regarding claims 10, 13-14, 29, and 41-43, Lin (Fig. 1C) further discloses that: the dielectric layer 126 extends beneath the chip 110 and the inner surface of the dielectric layer 126 faces upwardly toward the chip 110; the traces 136 are disposed on the inner side 124 and above the outer side 122 of the dielectric layer 126; and the bumps 138 extend at least partially through the dielectric layer 126 and have bottom ends 142 disposed below the outer surface 122 of the chip carrier.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
March 31, 2006

PHAT X. CAO
PRIMARY EXAMINER